PATENT
Attorney Docket No. SAM-0274

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Min-su Kim, et al.
Filing Date: Herewith
Title: SEMICONDUCTOR DEVICE HAVING SILICON-ON-INSULATOR STRUCTURE AND METHOD OF FABRICATING THE SAME

CERTIFICATE OF MAILING UNDER 37 C.F.R.§ 1.10

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11-26-01
Date

Amy Green

BOX PATENT APPLICATION
U.S. Patent and Trademark Office
P.O. Box 2327
Arlington, VA 22202

PRELIMINARY AMENDMENT

Sir:

Please amend the application as follows:

In the Specification

Please amend the specification as follows:

Please replace the paragraph at page 9 lines 14 through 26 with the following rewritten paragraph.

- - N^- type impurity ions are implanted into a region where n^+ type source and drain regions 130 and 140 will be formed, using the gate conductive layer 200 and mask layer pattern exposing both sides of the gate conductive layer 200 as ion implantation masks. After the mask layer pattern is removed, p^- type impurity ions are implanted into a region where a p^+ type body contact region 160 and an n^+ type source region 130 will be formed, using a mask layer pattern exposing one side of the region and the gate conductive layer 200 as ion implantation masks.

The mask layer pattern is removed and n^- type and p^- type impurity ions are diffused to form an n^+ type source region 130, an n^+ type drain region 140, and a p^+ type body contact region 160. An interlayer dielectric layer is formed, and then a portion thereof is etched to form a source contact hole 130c, a drain contact hole 140c, and a gate contact hole 200c. A source electrode 210, a drain electrode 220, and a gate electrode 230 are formed to fill the source, drain, and gate contact holes 130c, 140c, and 200c, respectively.

Applicant(s): Min-soo Kim, et al.

REMARKS

No new matter is added to the application. Entry is respectfully requested.

Attached hereto is a marked-up version of the changes made to the application by the current Amendment. The attached pages are captioned "Version with Markings to Show Changes Made."

Respectfully submitted,

Date: 11/26/01

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Version with Markings to Show Changes Made

In the Specification

The paragraph at page 9 lines 14 through 26 has been amended as follows:

- - N^{-} type impurity ions are implanted into a region where n^{+} type source and drain regions 130 and 140 will be formed, [using a mask layer pattern exposing both sides of the gate insulating layer 190 and the gate conductive layer 200] using the gate conductive layer 200 and mask layer pattern exposing both sides of the gate conductive layer 200 as ion implantation masks. After the mask layer pattern is removed, p^{-} type impurity ions_are implanted into a region where a p^{+} type body contact region 160 and an n^{+} type source region 130 will be formed, using a mask layer pattern exposing one side of the region and the gate conductive layer 200 as ion implantation masks. The mask layer pattern is removed and n^{-} type and p^{-} type impurity ions are diffused to form an n^{+} type source region 130, an n^{+} type drain region 140, and a p^{+} type body contact region 160. An interlayer dielectric layer is formed, and then a portion thereof is etched to form a source contact hole 130c, a drain contact hole 140c, and a gate contact hole 200c. A source electrode 210, a drain electrode 220, and a gate electrode 230 are formed to fill the source, drain, and gate contact holes 130c, 140c, and 200c, respectively. - -

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